Module and Application Description

PROCONTROL P

Binary and Analog Control Signal Processing

Control Module

for Binary Control Functions, 4-fold
for Analog Control Functions, 1- to 4-fold

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Application

The module is used for stored–program binary and analog control tasks on the drive, group, and unit control levels. It can be used for the following applications:

– Drive control for unidirectional drives
– Drive control for actuators
– Drive control for solenoid valves
– Binary function group control (sequential and logic control)
– 3–step control
– Signal conditioning

The module is intended for use in connection with the multi–purpose processing station.

The module is designed for three modes of operation:

– Binary control mode
(and analog basic functions)
with variable cycle time
– Analog control mode
(and binary control)
with fixed, selectable cycle time
– Signal conditioning mode
with fixed cycle time and disturbance bit output

The operating mode is selected by means of function block TXT1 which is the first function block required in the structure.

In the binary control mode, up to 4 binary function group controls, or combinations of drive and binary function group controls can be configured for each module (noting the module cycle time).

In the analog control mode, a maximum of 4 analog control loops in the form of 3–step controllers – depending on the actuating time of the actuator – can be configured for each module (see ”Operating modes”).

The module incorporates 4 hardware interfaces for the switchgear and/or the process.

Features

The module address is set automatically by plugging the module into the multi–purpose processing station.

The telegrams received via the station bus are checked by the module for error–free transfer based on their parity bits.

The telegrams sent by the module to the bus are given parity bits to ensure error–free transfer.

The user program is filed in a nonvolatile memory (EEPROM). It can be loaded and changed from the PDDS using the bus.

The module is ready for operation as soon as a valid user list is loaded.

For communicating with the process and the switchgear, the module requires the following voltage:

USA/USB Operating voltage +24 V
branched internally into the following voltages:
US11 Supply of contacts of process interface 1
US21 Supply of contacts of process interface 2
US31 Supply of contacts of process interface 3
US41 Supply of contacts of process interface 4

The voltages US11...US41 are short–circuit–proof and designed to prevent interaction.

Operating voltages and external logic signals are related to reference conductor Z.

The following annunciations are made on the front of the module by light–emitting diodes:

ST Disturbance
SG Module disturbance

Signal lamp ST signals any disturbance inside the module and of data communication with the module.
Signal lamp SG signals module disturbances only.

ASEA BROWN BOVERI

Module design

The module essentially consists of

– Process interfaces
– Station–bus interface
– Processing section

Process interfaces

In the process interfaces, the process signals are adapted to the module–internal signal level.

Station bus interface

In the station bus interface, the module signals are adapted to the bus. This essentially involves parallel/serial conversion.

Processing section

For processing the signals coming from the process and the bus, the module is equipped with a microprocessor which cooperates with the following memory areas using a module–internal bus:

Contents	Type of memory
Operating program	EPROM
Function blocks	EPROM
User program (structure, address, parameter, limit value, and simulation lists)	EEPROM
User program (structure, address, parameter, limit value, and simulation lists)	RAM
History values	RAM
Current module input and output signals (shared memory)	RAM

The operating program enables the microprocessor to perform the basic operations of the module.

The memory for the function blocks contains ready programs for implementing the various functions.

The function blocks available in a particular operating mode are selected in such a way that the specified task can be performed without additional modules required. For instance, in the analog control mode, it is possible to set up a superposed setpoint control in addition to the single–variable analog control.

All function blocks and their inputs and outputs can be called by the user via the programming, diagnostic and display system (PDDS).

The memory for the user program contains information as to:

– how the function blocks are interconnected,
– which module inputs and outputs are assigned to which inputs and outputs of the function blocks,
– which fixed values are specified for the individual inputs of the function blocks,
– which parameters are specified for the individual inputs of the function blocks,
– which plant signals are assigned to the individual module inputs and outputs,
– which function blocks serve the process interfaces,
– which sets of limit values are allocated to the analog values,
– which module input signals are simulated.

These data are specified by the user depending on the specific plant requirements.

For normal operation, the complete user program is filed in an EEPROM. For optimization purposes, it is possible to work with a modified copy of the user program in the RAM, which must then be taken over into the EEPROM upon completion of the optimizing process.

Settings (mainly for analog control applications) can either be preset by the user directly at the appropriate function block inputs or alternatively specified in a separate parameter list.

If limit signals are generated by function block GRE, the limit values (4 per GRE) are specified in a limit value list.

Parameter and limit value lists can be changed (on line) at any time during operation. For this purpose, they are stored in the RAM or the EEPROM, depending on their allocation to the RAM or EEPROM mode respectively.

Data exchange between module and bus system takes place through the memory for module input and output signals. It is used for buffering the signals.

Structuring

For structuring purposes, the neutral inputs and outputs of the individual function blocks are assigned certain module inputs and outputs, or the inputs of the function blocks are given fixed values and parameters or outputs of other function blocks (calculated function results). Structuring is performed on the basis of the data supplied by the user in the form of a so–called structure list.

Structuring is to be carried out considering the following limit values of the module:

– max. number of module inputs	287
– max. number of simulatable module inputs	32
– max. number of module outputs	223
– max. number of calculated function results	255
– max. number of timers	128
– max. number of parameters	80
– max. number of limit value sets	16
– max. number of drive control functions (binary control, analog control) e.g. ASE, ASS, ASM and ASI functions	4
– max. number of group control functions e.g. GSA and GSV functions	4
– max. number of lines in structure list	2917
– length of history value list (bytes)	768
– Size of shared memory (see “Addressing”)	

Here, one line stands for one entry on the PDDS.

The proper procedure to be followed for structuring the function blocks is explained in the Function Block Descriptions.

Addressing

General

Signal exchange between module and bus system takes place through a shared memory. This memory buffers arriving telegrams, which are to be received by the module, as well as calculated function results which are to leave the module.

For this reason, the shared memory uses source registers for the telegrams to be sent and sink registers for telegrams to be received. Register numbers 0 to 63 are defined as source registers and register numbers 64 to 199 are defined as sink registers.

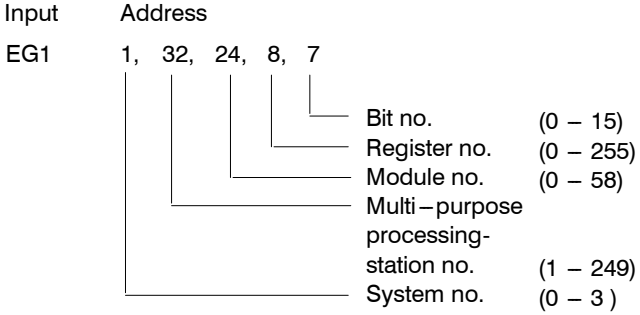
The allocation of module input and output signals to the respective registers of the shared memory is determined by user data entered via the PDDS.

The user entries are made in the form of address lists.

Address list for module inputs

In the address list for module inputs, each module input is assigned the source location or the associated process interface of the signal to be received.

For module inputs receiving their signals from the bus, addressing is done by allocating the source location address to EGn, e.g.:



For module inputs receiving their signal from the process interface, addressing is done by allocating the process interface to EGn, e.g.:

For module inputs receiving their signal from the process operator station (POS), addressing is done by allocating L to EGn, e.g.:

The address list for inputs is translated by the PDDS into two module–internal lists, the ”Bus address list” and the ”Allocation list Module inputs”.

For all telegrams to be used by the module, the bus address list contains the respective source addresses and sink registers.

Incoming telegrams whose addresses are included in the bus address list are written into the sink register of the shared memory. Incoming telegrams whose addresses are not included in the bus address list are ignored by the module.

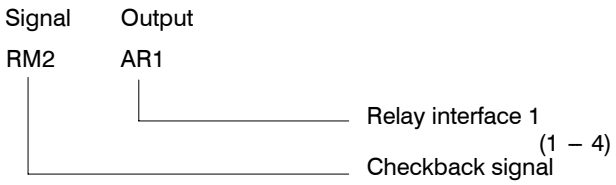
The allocation list for module inputs includes, for each module input, the associated sink register number and, in the case of binary values, also the bit position.

Address list for module outputs to the bus

In the address list for module outputs, a source register is defined for each signal to be issued by the module. Additionally, a source bit is defined in the case of binary signals, e.g.:

Addressing the process interface for the relay outputs

For module outputs supplying their signal to the relay interface, addressing is done in the structure list by allocating ARn, n denoting the number of the relay interface, e.g.:



Address formation

The system and station addresses are set on the station–bus control module and are transmitted by this module to all other modules belonging to one multi–purpose processing station.

The module addresses are defined by the connections made on the backplane so that each module is automatically set to the assigned address when being plugged into its slot.

Limit value list

The limit value list contains a set of 4 limit values for each one of a maximum of 16 function blocks GRE (limit signal formation for one analog value). It is stored in the EEPROM and – in the case of RAM operation – in the RAM.

Limit value lists can be changed at any time from the PDDS and POS using a ”job memory” (RAM). Changes are stored in the EEPROM in the case of EEPROM operation, and in the RAM in the case of RAM operation. When user lists are taken over from the RAM into the EEPROM, and vice versa, the limit value lists are also taken over.

Parameter list

The parameter list contains up to 80 values for parameters of the function blocks. It is handled and stored in the same way as the limit value list.

Simulation list

Using the PDDS, it is possible to simulate, at up to 32 module inputs, signals normally received via the bus, by overwriting them with constant values. This simulation list is handled and stored in the same way as the limit value list.

Event generation

The module is requested by the PROCONTROL system once every cycle to transmit the information filed in the source registers of the shared memory.

If any values change during a cycle, this change will be treated as an event.

The module recognizes the following occurrences as events:

– Change of status in the case of binary values
– Change of an analog value by a permanently set threshold value of approx. 0.39 % and elapse of a time delay of 200 ms since the last transfer (cyclic or event–related).

If an event occurs, cyclic operation is interrupted and the new values are transferred to the bus with priority.

Disturbance bit evaluation, reception monitoring

The telegrams supplied via the bus may be provided with a fault flag on bit position 0. This fault flag is generated by the source module on the basis of plausibility checks, and the disturbance bit is set to “1” in the event that specific disturbances are present (see Function Block Descriptions).

In order to be able to recognize errors during signal transfer, the module also incorporates a feature that monitors the input telegrams for cyclic renewal. If a telegram has not been renewed within a certain time (e.g. due to failure of the source module), bit 0 is set to ”1” in the allocated sink register of the shared memory. In binary value telegrams, all the binary values are simultaneously set to “0”. In the case of analog values, the previous value is retained.

A set disturbance bit does not automatically involve a reaction in the sink module. If the disturbance bit of a telegram is to be evaluated, provision must be made for this during structuring.

In the ”Binary control” and ”Analog control” modes, disturbance bits of received telegrams can only be used within the module. They are not included in telegrams which are to be transmitted.

In the ”Signal conditioning” mode, disturbance bits are also included in transmitted telegrams.

Diagnosis and annunciation functions

Disturbance annunciations on the module

The light–emitting diodes on the module front are used for the following annunciations:

	Designation of LED
– Disturbance	ST
– Module disturbance	SG

Light–emitting diode ST signals all disturbances of the module and of data communication with the module.

Light–emitting diode SG signals module disturbances only.

Disturbance annunciation signals to the alarm annunciation system

The alarm annunciation system and the control diagnostic system (CDS) receive disturbance annunciation signals from the control module via the bus.

Diagnosis

The incoming telegrams, the generation of telegrams to be transmitted, and internal signal processing are monitored for errors in the processing section of the module (self–diagnosis).

In the event of a disturbance, the type of disturbance is filed in the diagnostic register and, at the same time, a general disturbance annunciation is signalled to the PROCONTROL system.

When prompted, the module transfers a telegram containing the data stored in the diagnostic register (register 246) (see Fig.1).

The contents of the diagnostic register, the annunciations signalled via the general disturbance line, the annunciations on the CDS, and annunciation ST are shown in Fig. 1.

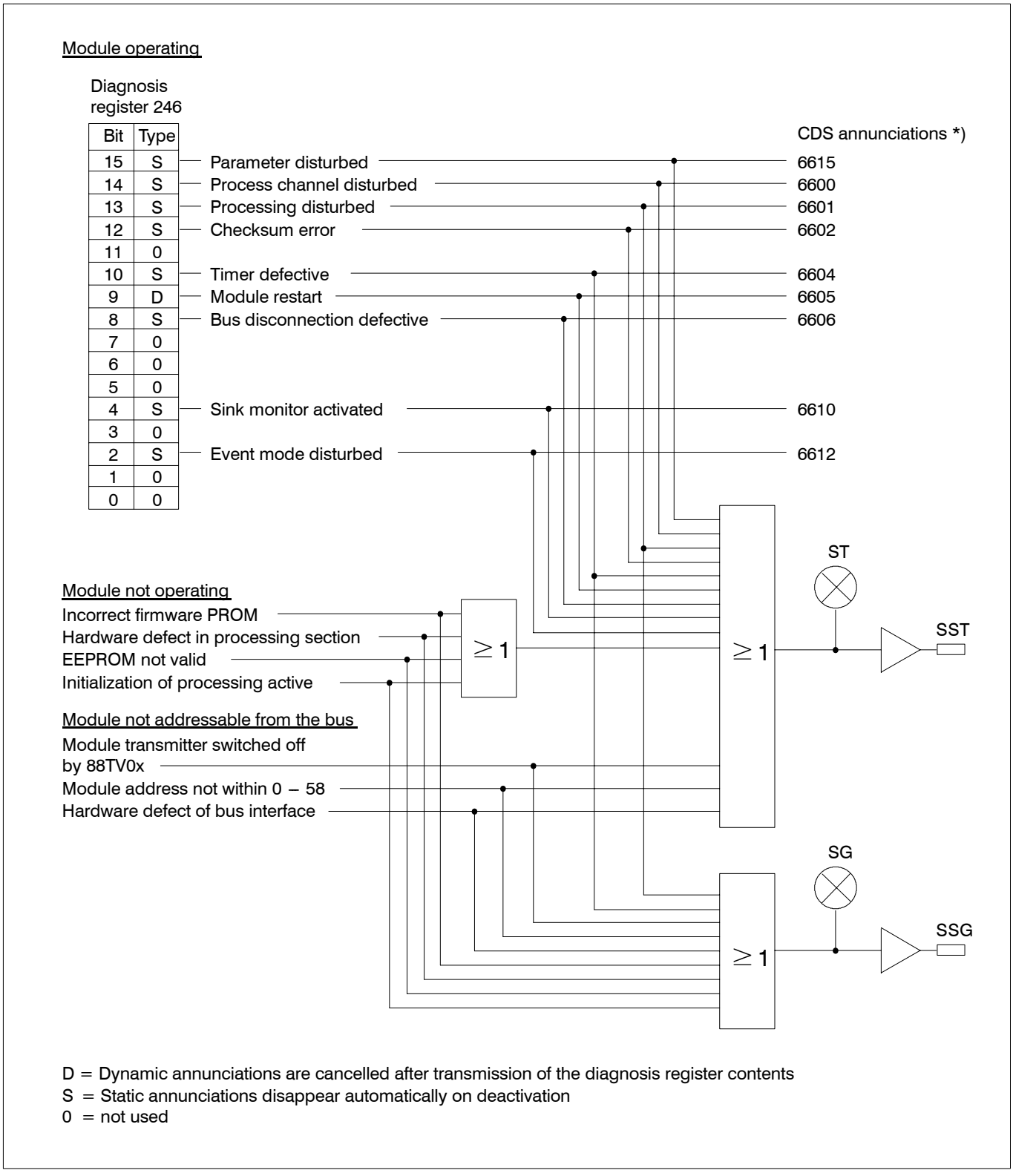


Figure 1: Diagnostic annunciations of 83SR04

The annunciation ”Process channel disturbed” may appear for the following reason:

– Short circuit at outputs US11...US41

*) The control diagnostic system (CDS) provides a description for every annunciation number. This description provides, among other data:

– Information on cause and effect of the disturbance
– Recommendations for its elimination.

This makes for fast elimination of disturbances.

Operating statuses of the module

Initialization and bootstrapping with user lists

Initialization is accomplished either by plugging the module into its slot or after connecting the voltage.

The initialization process causes the module to assume a defined initial state. Light–emitting diodes ST and SG are lit during this process.

No user program is available when the module is started up for the first time. As a result, the module signals ”Processing disturbed”, and the light–emitting diodes ST and SG are on.

As a first step, it is necessary to transfer the user program from the PDDS, via the bus, to the RAM of the module. If this operation is started with the structure list, PDDS calls all other lists automatically. To avoid the transmission of incorrect lists, the PDDS checks the location and the address before each transmission job. The module checks every incoming list for plausibility.

Now, the complete user program can be transferred to the EEPROM by a PDDS command.

Following this, the module is ready for operation, and the light–emitting diodes ST and SG are deenergized.

Normal operation

The module processes the user program filed in the EEPROM.

In normal operation, the signals arriving from the bus and the process interface are processed in accordance with the instructions contained in the structure list.

In line with these instructions, commands are output to the switchgear, and checkback signals indicating the process status are transmitted via the bus.

Modification of parameter and limit value lists

Parameters and limit values can be changed from the PDDS and, if they have been configured using the POS, from the POS (see ”Limit value list” and ”Parameter list”).

Modification of structure and address lists

Structure and address lists can be transferred to the PDDS, modified there and transferred back to the module. To do so, the following procedure should be followed:

– The module should be in the EEPROM mode,

– copy the complete user program from the EEPROM to the RAM using PDDS command ”COP”,

– transfer the list to be changed from the EEPROM (or RAM) to the PDDS and modify it,

– transfer the modified list to the module, thus, effecting automatic storage in the RAM

– switch the module from EEPROM operation over to RAM operation by using PDDS command ”SWI”, and test the new list,

– to make further changes, switch again to EEPROM operation, repeat procedure.

Upon successful completion of the test, the complete user program can be transferred from the RAM to the nonvolatile EEPROM, using either of the following commands:

– PDDS command ”Save” (SAV) or

– PDDS commands ”Copy from RAM to EEPROM” (COP) and ”Switch over from RAM to EEPROM” (SWI)

The ”Save” command effects copying of the lists and subsequent automatic switchover to EEPROM, impairing neither processing on the module nor command output.

Following a switchover operation with command SWI (from RAM to EEPROM and from EEPROM to RAM), the user lists in the RAM and EEPROM are compared. Should any deviation be detected, the controllers and the binary group controls are switched to ”Manual”, memories and timers are reset, and the commands present at the process interface are deactivated. For changed addresses of module inputs (EGn), the associated entries in the shared memory are set to zero until new data are received for the first time after switchover.

Simulation

The PDDS permits constant values to be specified to the module for a maximum of 32 individual module input signals which in normal operation arrive from the transfer system. In this case, the sink registers entered in the allocation list for module inputs are overwritten by constants. These simulation data and the previously entered sink register numbers are stored in the EEPROM in the case of EEPROM operation, or in the RAM in the case of RAM operation.

The simulation data are also copied when the user lists are transferred from the RAM to the EEPROM, and vice versa.

On cancellation of a simulation process via the PDDS, the sink register number is written back into the allocation list, and the module continues to operate with the value transferred by the bus.

Command functions

Actuation from the control room

The module does not incorporate control room interfaces.

Actuation by a higher–level automatic system

A higher–level automatic system actuates the module via the bus.

Release and protective commands

The logic combinations for release and protective commands are specified as required for the plant involved.

Command output

The commands for the drive control functions (binary control or step control), to which the process interfaces were assigned, are output via relay outputs B11/B12 ...B41/B42. In conjunction with order outputs BV1...BV4, common to both command outputs, the relay outputs above actuate coupling relays on a two–channel basis.

The voltage for the command outputs B11/B12... B41/B42 is derived for each function unit from a separate, module–internal voltage.

The outputs are short–circuit–proof, protected against mutual interference, and provided with a protective circuit.

Checkback signals from the process

The drive–related checkback signals from the process are connected in the case of the drive control functions, to the hardware inputs of the module (see "Function diagram" and/or "Connection diagrams").

Operating modes

The module incorporates all function blocks required for the binary control, analog control, and signal processing tasks on the drive, group, and unit control levels. A set of function blocks is specified as "Operating mode" for a particular application. This is done by means of function block TXT1 which must appear at the top of the structure list. Next follow the TXT text elements for main function as well as function designations, and for processing functions.

Operating mode	Module cycle time	Input TXT1
Binary control (and analog basic functions)	variable up to max. 700 ms	STR
Analog control (and binary control)	fixed: 50, 100 150, 200 or 250 ms	REG, x x = 50 ms x = 100 ms x = 150 ms x = 200 ms x = 250 ms
Signal conditioning with disturbance bit output	fixed: 250 ms	MWV

The module cycle time is determined by number and type of the function blocks entered in the structure list. The cycle times indicated as "fixed" are minimum times. They apply whenever the time resulting from the structure list is shorter.
The actually required time is filed in register 205 and can be read out from the PDDS.

The following set of functions can be implemented for each module:

– 4 group control functions, e.g. GSA/GSV functions or
– 4 drive control functions, e.g. ASI/ASE/ASS/ASM functions or
– combinations of drive and group controls are permissible. The cycle time of the module has to be taken into account.

Depending on the module cycle time chosen, the following combinations are possible in the analog control mode:

Operating mode **Analog control** (and binary control)	REG 50 ms	REG 100 ms		REG 150 ms			REG 200/ 250 ms			
ASI	1	1	2	1	2	3	1	2	3	4
ASE, ASM, ASS	–	≤ 3	–	≤ 3		–	≤ 3			–

The cycle time of the module has to be taken into consideration.

The 4 process interfaces of the module including command outputs are assigned to the drive control functions ASE/ASS/ASM/ASI whose inputs for process annunciation (PRO) are marked "VPn" in the address list. The following assignments apply:

n = 1 Process interface 1
n = 2 Process interface 2
n = 3 Process interface 3
n = 4 Process interface 4

The module is connected to the control room through the process operator station.

Function blocks for the binary control mode (STR)

This operating mode provides the function blocks for all binary control functions on the drive, group and unit control levels. Additional analog basic functions are available.

The module cycle time is variable, i.e. it is strictly determined by the function blocks used.

In this operating mode, no disturbance bits are transmitted, except in the standard checkback telegrams.

Function blocks	**Abbrev.**
BINARY FUNCTIONS	
Switch–off delay element	ASV
2–out–of–3 selection, binary	B23
2–out–of–4 selection, binary	B24
M–out–of–N selection	BMN
Extended bit marshalling	BRA1
Dual–BCD converter	DBC1
Dual–decimal converter	DDC
Dynamic OR gate	DOD
Switch–on delay element	ESV
Monostable flipflop ”Break”	MOA
Monostable flipflop ”Constant”	MOK
OR gate	ODR
RS flipflop	RSR
AND gate	UND
Counter	ZAE
GROUP CONTROL	
Group control function for sequential control	GSA2
Group control function for sequential control	GSV
Criteria call	KRA1
Criteria call without watchdog	KRA3
Step function	SCH1
Preselect function, 2–fold	VW2
Preselect function, 3–fold	VW3
Preselect function, 4–fold	VW4
Selector switch, 4–fold	WS4
DRIVE CONTROL	
Drive control function for unidirectional drive	ASE1
Drive control function for solenoid valve	ASM1
Drive control function for actuator	ASS1

Function blocks	**Abbrev.**
LIMIT SIGNAL ELEMENTS	
Limit signal element for upper limit value	GOG
Limit signal element for lower limit value	GUG
Limit signal generation	GRE
ANALOG FUNCTIONS	
Absolute value generator	ABS
Limiter	BEG
Divider	DIV
Function generator	FKG
Factor variation	KVA
Maximum value selector	MAX
Minimum value selector	MIN
Multiplier	MUL
Monitoring and select function	MVN
Delay element, first order	PT1
Square–root extractor	RAD
Summing multiplier	SMU
Disturbance bit suppression	SZU
Time variation	TVA
Changeover switch	UMS
PUSHBUTTON SELECTION FUNCTIONS	
Pushbutton selection	TAW
Pushbutton selection incl. target value presetting	TAZ
ORGANIZATION FUNCTIONS	
Text element for designation and note	TXT
Text element for operating mode indication	TXT1

The exact specification of the function blocks as well as the procedure for structuring are shown in the function block descriptions.

Function blocks for the analog control mode (REG)

This operating mode uses the function blocks for all analog control functions for single–variable and master control. In addition, the function blocks for drive and group control are available.

In this operating mode, no disturbance bits are transferred, except in the standard checkback signals.

The module cycle time can be preset in steps as a fixed minimum time (see entries in text element TXT1).
When implementing several control loops on a certain module, it should be noted that the cycle time of the module increases accordingly.

To ensure precise positioning in the case of single variable step controllers, the actuating time of the actuator (from 0 – 100 %) must correspond to 200 times the module cycle time, e.g.

Actuating time > 10 s at a cycle time of 50 ms

Function block	**Abbrev.**
BINARY FUNCTIONS	
Switch–off delay element	ASV
2–out–of–3 selection, binary	B23
2–out–of–4 selection, binary	B24
M–out–of–N selection	BMN
Extended bit marshalling	BRA1
Dual–BCD converter	DBC1
Dual–decimal converter	DDC
Dynamic OR gate	DOD
Switch–on delay element	ESV
Monostable flipflop, ”Break”	MOA
Monostable flipflop, ”Constant”	MOK
OR gate	ODR
RS flipflop	RSR
AND gate	UND
Counter	ZAE
DRIVE CONTROL	
Drive control function, unidirectional drive	ASE1
Drive control function, incremental output with extended capabilities	ASI2
Drive control function, solenoid valve	ASM1
Drive control function, actuator	ASS1
LIMIT SIGNAL ELEMENTS	
Limit signal element for upper limit value	GOG
Limit signal generation	GRE
Limit signal element for lower limit value	GUG

Function block	**Abbrev.**
ANALOG FUNCTIONS	
Absolute value generator	ABS
Limiter	BEG
Divider	DIV
Function generator	FKG
Integrator	INT
Factor variation	KVA
Maximum value selector	MAX
Minimum value selector	MIN
Multiplier	MUL
Monitoring and select function	MVN
Differentiator with derivative action	PDT
Delay element, first order	PT1
Square–root extractor	RAD
Summing multiplier	SMU
Time variation	TVA
Changeover switch	UMS
ANALOG CONTROL	
Manual station	HST
PID controller	PID1
PI controller	PIR1
P controller	PRE
Differentiator with derivative action time	PTV
Setpoint integrator	SWI
Setpoint adjuster	SWV1
Disturbance bit suppressor	SZU
PUSHBUTTON SELECTION FUNCTIONS	
Pushbutton selection	TAW
Pushbutton selection with target value presetting	TAZ
ORGANIZATION FUNCTIONS	
Text element	TXT
Text element for operating mode indication	TXT1

The exact specification of the function blocks as well as the procedure for structuring are shown in the function descriptions.

Function blocks for the signal conditioning mode (MWV)

This operating mode provides analog computing functions and basic binary functions. A separate complete function block "ENT" is available to calculate the enthalpy value. In addition, binary and analog control functions are available.

In this operating mode, any disturbance bits set to "1" in incoming telegrams are taken over into data telegrams, which have been calculated from these, and are then transmitted.

The minimum module cycle time is permanently set to 250 ms.

Function block	**Abbrev.**
BINARY FUNCTIONS	
Switch–off delay element	ASV
2–out–of–3 selection, binary	B23
2–out–of–4 selection, binary	B24
M–out–of–N selection	BMN
Extended bit marshalling	BRA1
Dual–BCD converter	DBC1
Dual–decimal converter	DDC
Dynamic OR gate	DOD
Switch–on delay element	ESV
Monostable flipflop (break)	MOA
Monostable flipflop (constant)	MOK
OR gate	ODR
RS flipflop	RSR
AND gate	UND
Counter	ZAE
LIMIT SIGNAL ELEMENTS	
Limit signal element for upper limit value	GOG
Limit signal generation	GRE
Limit signal element for lower limit value	GUG

Function block	**Abbrev.**
ANALOG FUNCTIONS	
Absolute value generator	ABS
Limiter	BEG
Divider	DIV
Enthalpy function	ENT
Function generator	FKG
Integrator	INT
Factor variation	KVA
Maximum value selection	MAX
Minimum value selection	MIN
Multiplier	MUL
Monitoring and select function	MVN
Differentiator with P–DT1 action	PDT
Delay element, first order	PT1
Differentiator with derivative action time	PTV
Square–root extractor	RAD
Summing multiplier	SMU
Time variation	TVA
Changeover switch	UMS
ORGANIZATION FUNCTIONS	
Text element	TXT
Text element for operating mode indication	TXT1

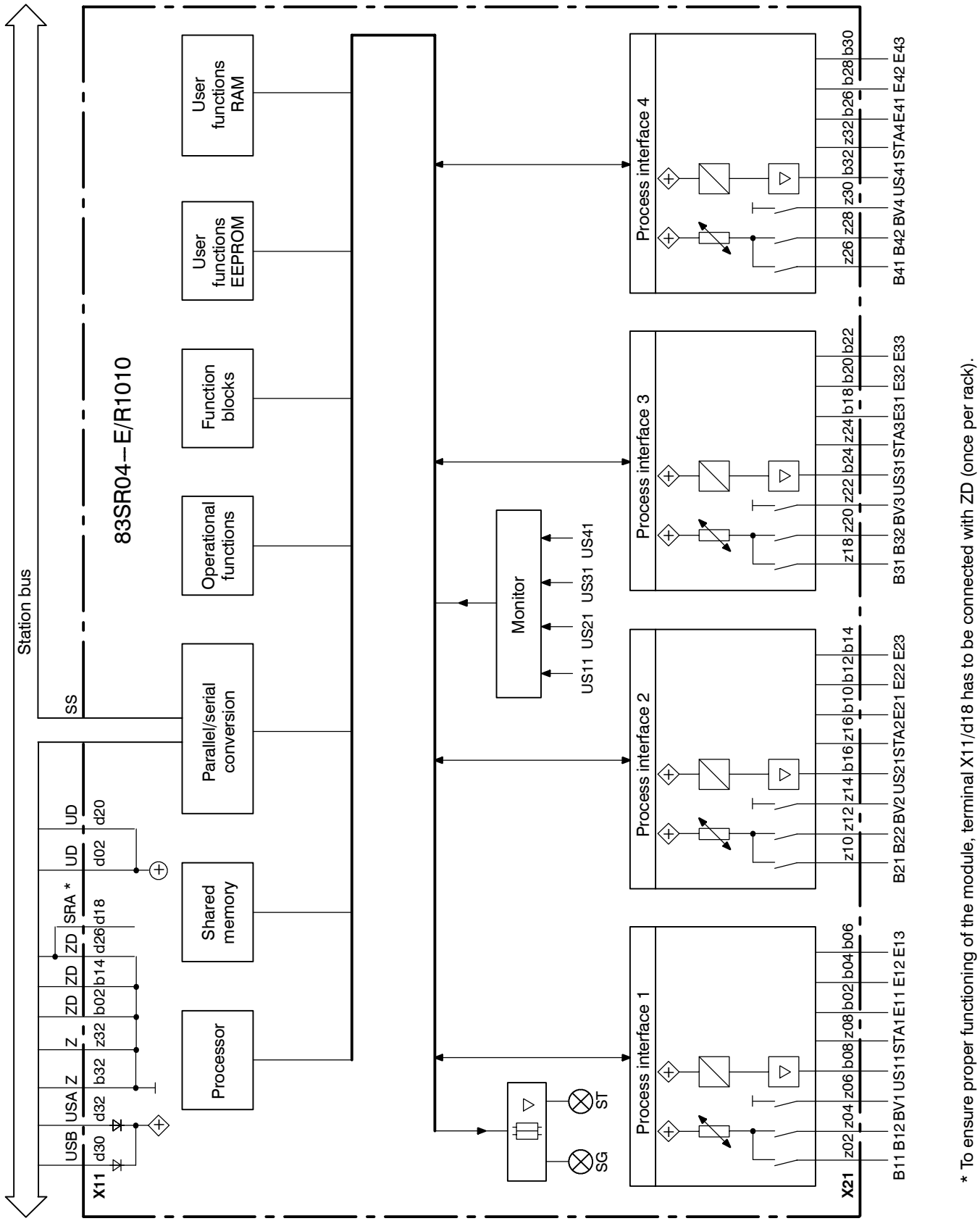
The exact specification of the function blocks as well as the procedure for structuring are shown in the function block descriptions.

Function diagram

Terminal designations

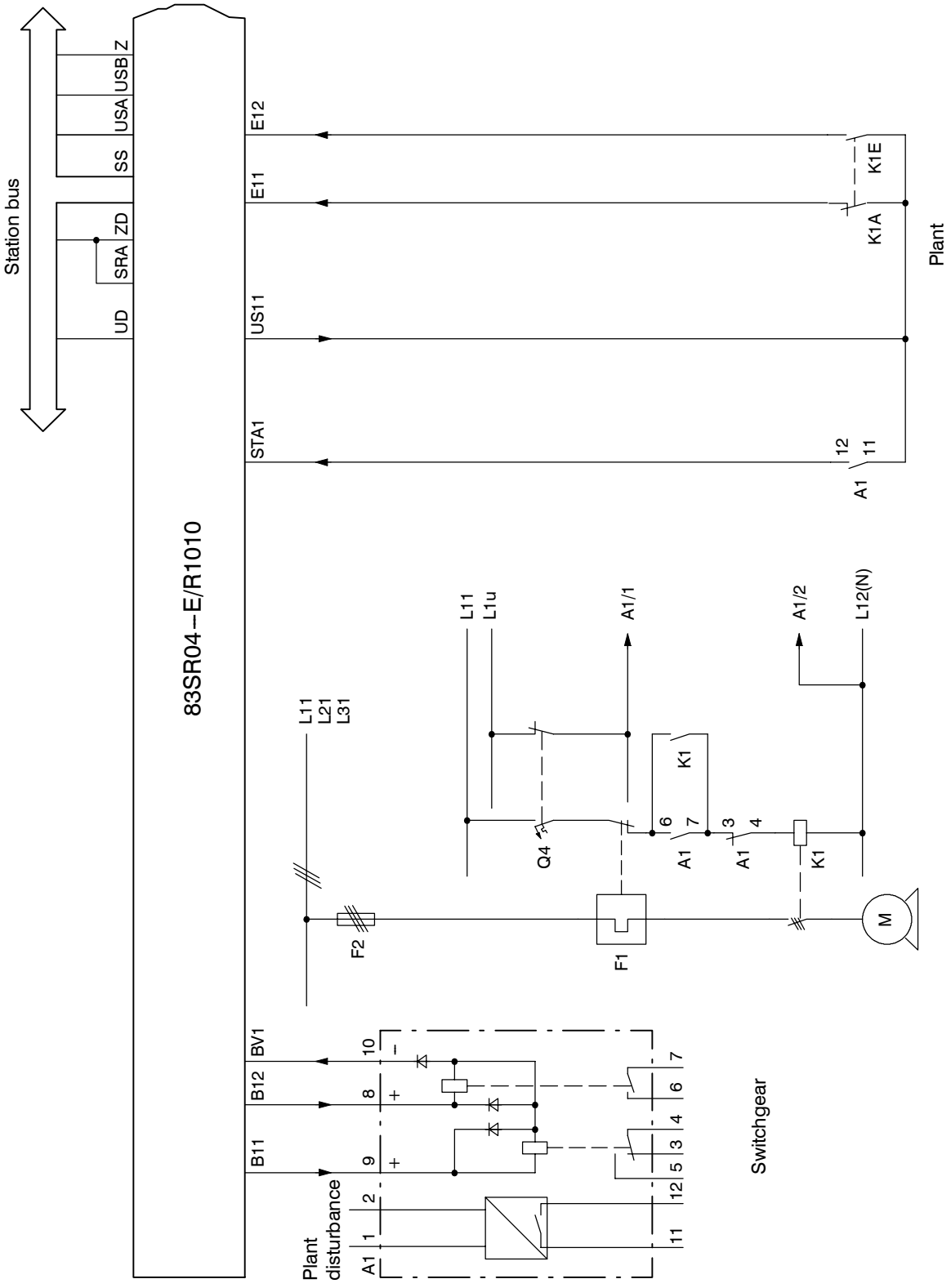
The printed–circuit board is equipped with connectors X11 and X21.

Connector X21 incorporates all process inputs and outputs. Connector X11 contains the station–bus interface and the operating voltages USA, USB and UD+.

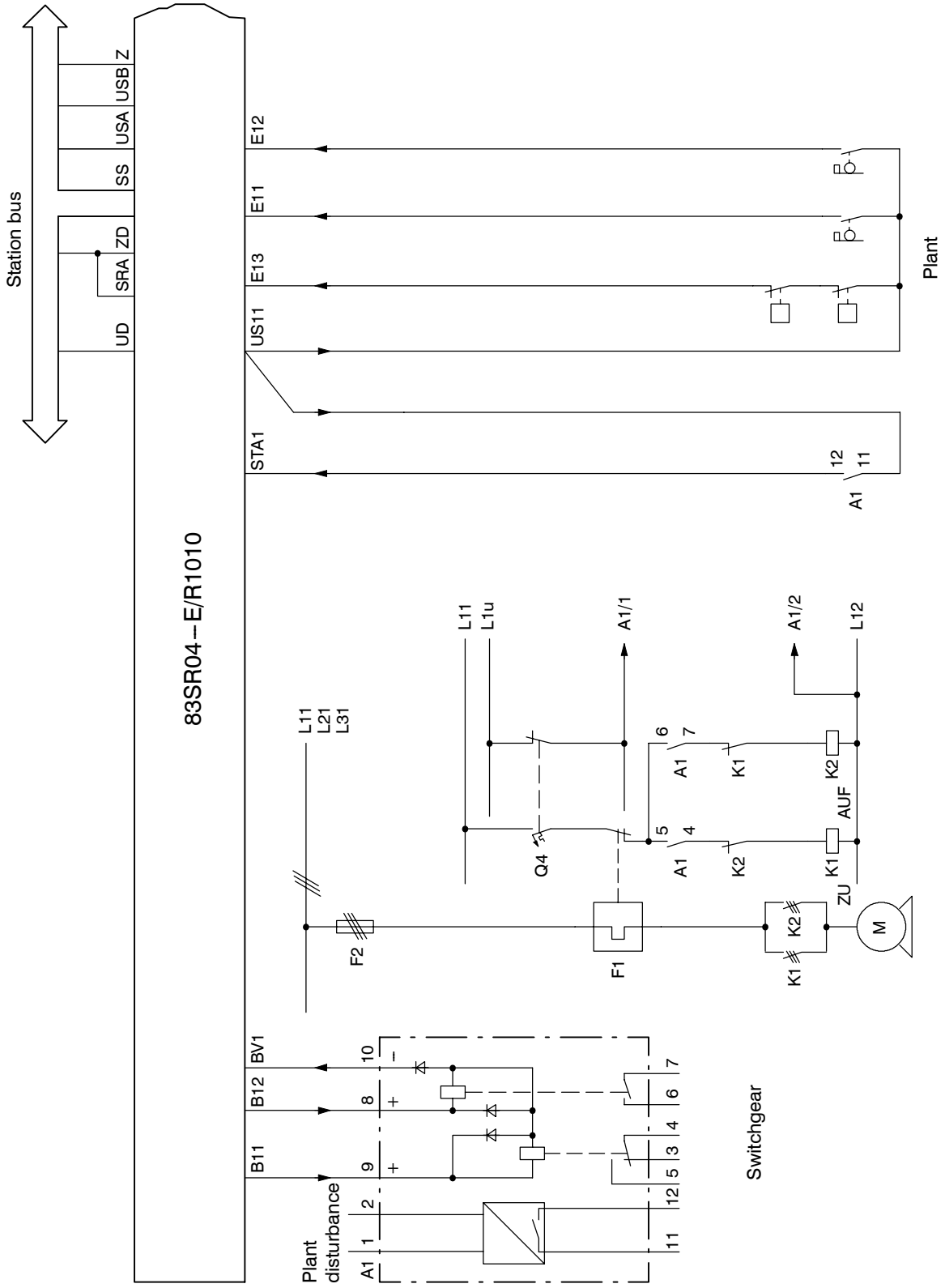


* To ensure proper functioning of the module, terminal X11/d18 has to be connected with ZD (once per rack).

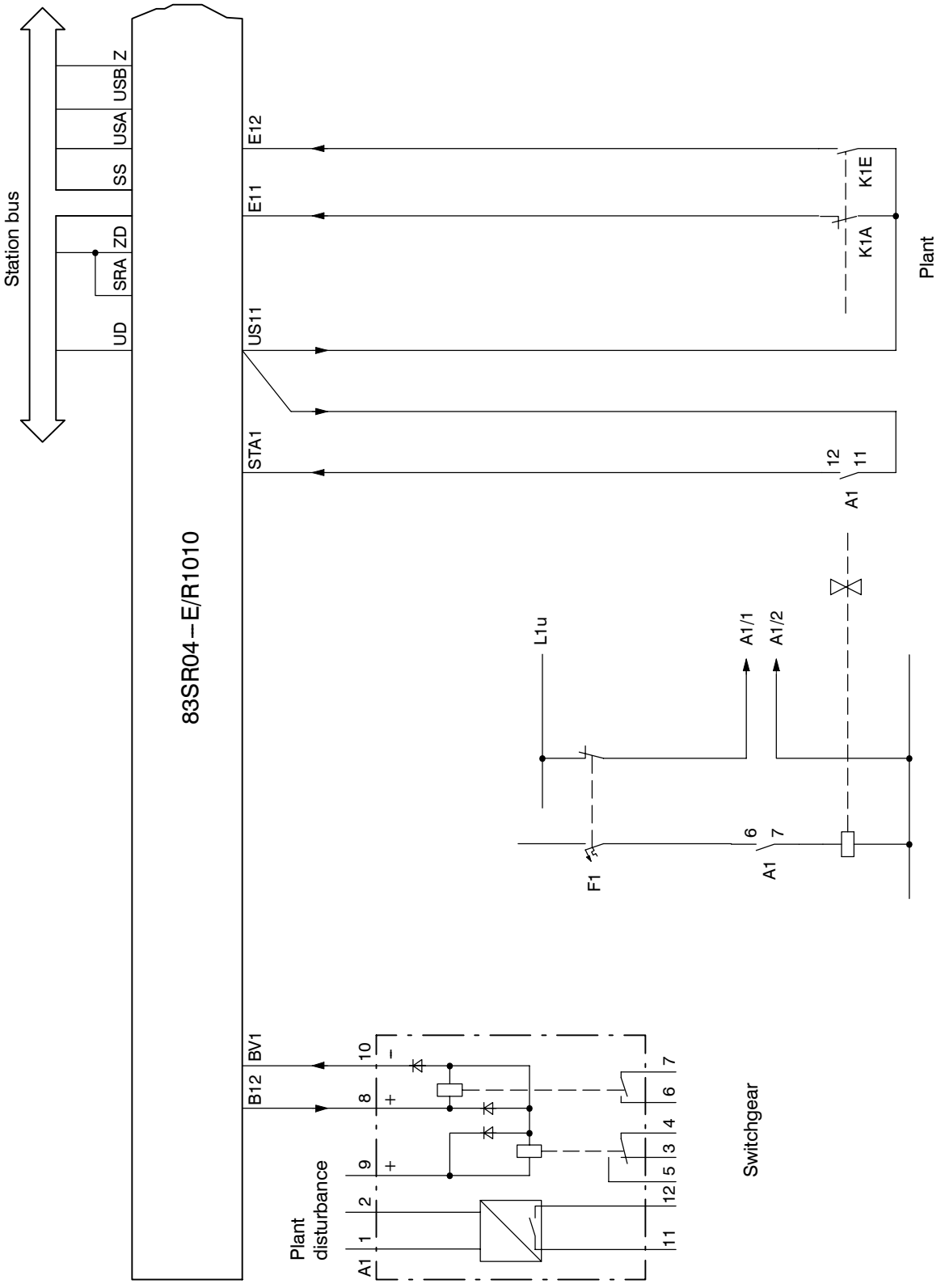
Connection diagram for unidirectional drive (function unit 1)



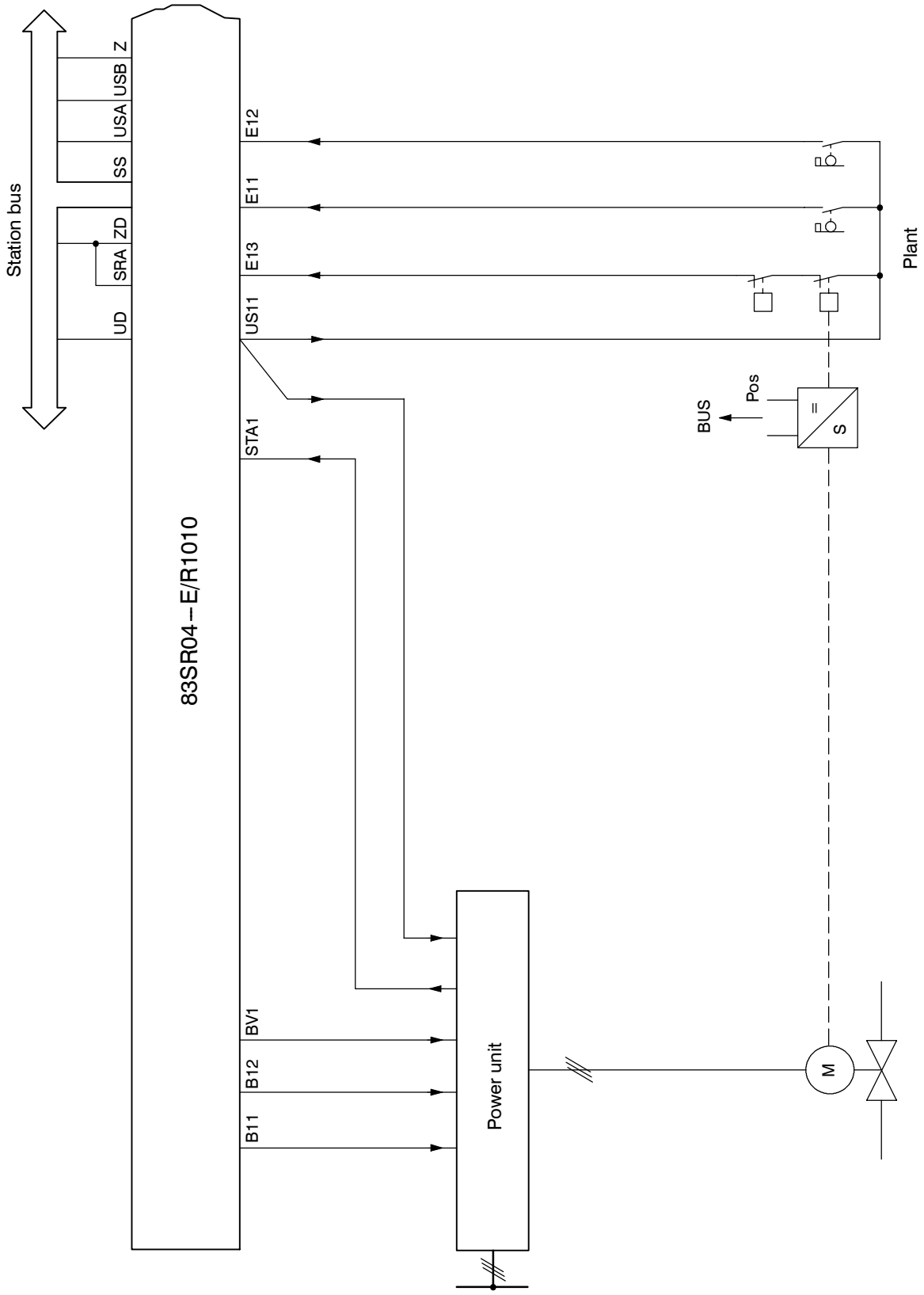
Connection diagram for actuator (function unit 1)



Connection diagram for solenoid valve (function unit 1)



Connection diagram for 3−step controller (function unit 1)



Mechanical design

Board size: 6 units, 1 division, 160 mm deep

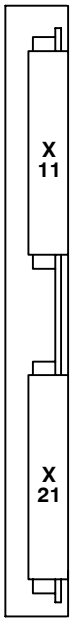
Connector: to DIN 41 612

1 x for station bus connection,
48–pole, edge–connector, type F
(connector X11)

1 x for process connection,
32–pole, edge–connector, type F
(connector X21)

Weight: approx. 0.55 kg

View of the connector side:



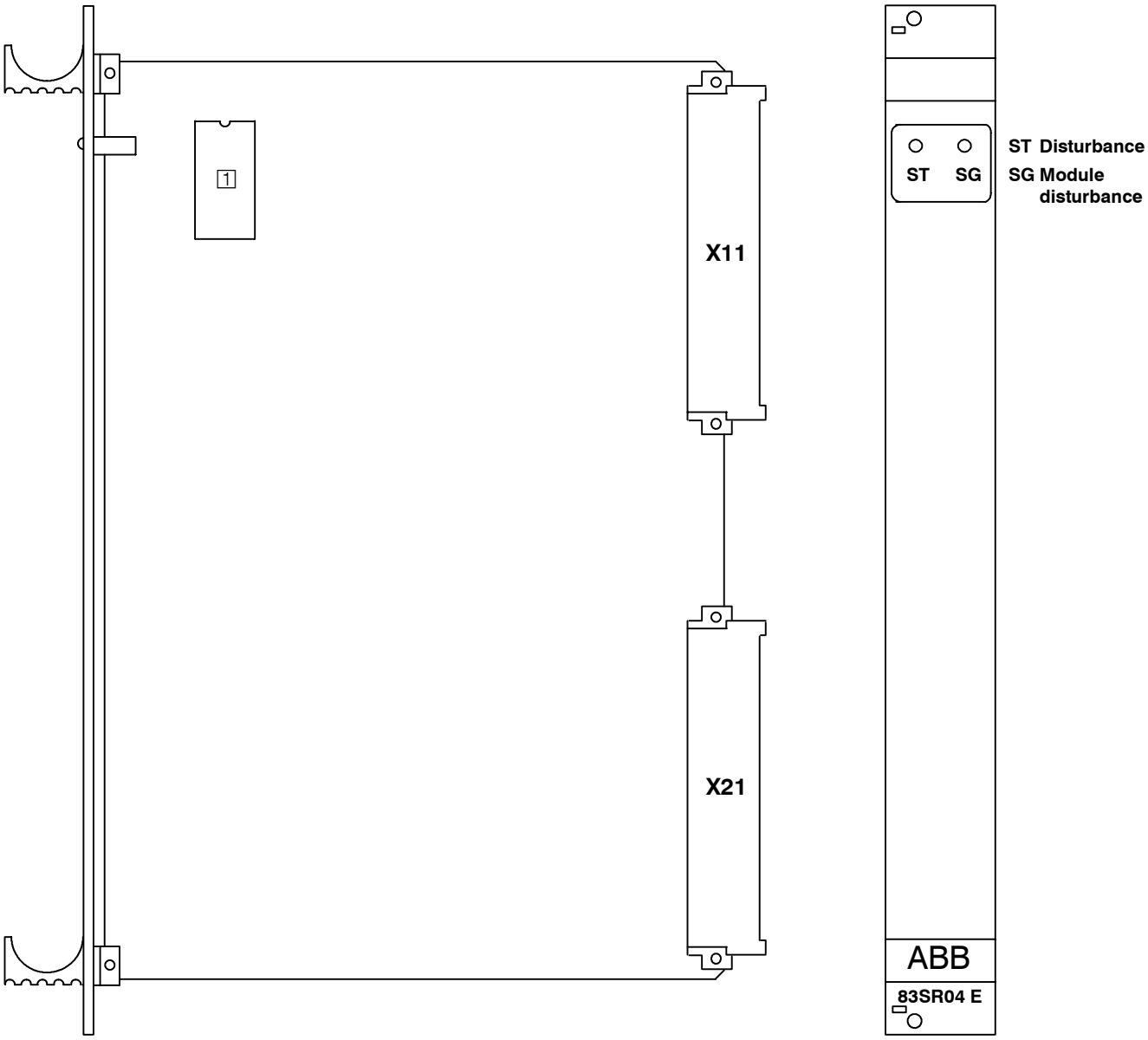
Side view and view of module front

Contact assignments of process connector X21

View of the contact side:

	b	*z*
02	E11	B11
04	E12	B12
06	E13	BV1
08	US11	STA1
10	E21	B21
12	E22	B22
14	E23	BV2
16	US21	STA2
18	E31	B31
20	E32	B32
22	E33	BV3
24	US31	STA3
26	E41	B41
28	E42	B42
30	E43	BV4
32	US41	STA4

[1] EPROM, programmed, order number: GJR2390241Pxxxx
xxxx = Position number as per applicable revision status


1
X11
X21
ST
SG
ST Disturbance
SG Module disturbance
ABB
83SR04 E

Technical data

In addition to the system data, the following values apply:

Power supply

Operating voltage of module		USA/USB = 24 V
Current consumption		IS = 80 mA + output currents
Operating voltage of bus section		UD = 5 V
Current consumption		ID = 250 mA
Power dissipation		PV = 3.5 W
Reference potential of process section		Z = 0 V
Reference potential of bus section		ZD = 0 V

Input values

Direct connections for 4 function units (FE)

Ex1 – Process checkback signal (EA/EZ)	OFF/CLOSED	5 mA at 48 V
Ex2 – Process checkback signal (EE/EO)	ON/OPEN	5 mA at 48 V
Ex3 – Torque monitor	CLOSED/OPEN	5 mA at 48 V
STAx – Disturbance in switchgear		5 mA at 48 V

x from 1 to 4

Output values

CONTACT VOLTAGES

Contact voltages of process section	US11 = 48 V / $\leq$ 30 mA
for inputs Ex1, Ex2, Ex3, and STAx	US21 = 48 V / $\leq$ 30 mA
	US31 = 48 V / $\leq$ 30 mA
	US41 = 48 V / $\leq$ 30 mA

x from 1 of 4

The outputs are short–circuit–proof and non–interacting.

PROCESS INTERFACE

Voltage supply of the 4 function units for command outputs Bx1 and Bx2		24 V
The outputs are short–circuit–proof and non–interacting, and are provided with a protection circuit		
		Loading capacity
Bx1 – Command output for	OFF/CLOSED	IS $\leq$ 80 mA
Bx2 – Command output for	ON/OPEN	IS $\leq$ 80 mA
BVx – Common command output for Bx1/Bx2 (wired return line)		IS $\leq$ 80 mA
Regarding the connected load resistor the following limits apply		360 $\Omega \leq R_{load} \leq$ 15 kΩ
Service life of the relay output stages		$\geq$20 million switching cycles

COUPLING RELAYS AND POWER DRIVERS IN THE SWITCHGEAR

Wiring:

The wiring from the 83SR04 to the switchgear is defined in a cable specification to suit the plant–specific requirements. The max. length of the line (outgoing plus return line) is 600 m for a cross–section of 0.5 mm^2.

The following coupling relays and power drivers may be used:

Coupling relay	R513
Power drivers with semiconductors or coupling relays or power drivers with identical technical data.	LU370

ORDERING DATA

Order number for complete module:

Type designation: 83SR04 – E/R1010 Order number: GJR2390200R1010

Technical data subject to change without notice!

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